CLAIMS

What is claimed is:

1. A computer system comprising:

a backplane that includes:

multiple sockets;

a bus that couples the multiple sockets together,

wherein the bus includes a capability signal line; and

a circuit board inserted in one of the multiple sockets, and configured to limit a voltage on the capability signal line to one of three or more predetermined values, wherein the predetermined values are indicative of different bus component capability levels.

2. The system of claim 1, wherein the predetermined values are indicative of a maximum bus clock rate supported by the circuit board.

3. The system of claim 1, wherein the circuit board includes a voting circuit that limits the voltage on the capability signal line when the voting circuit is enabled.

4. The system of claim 3, wherein the voting circuit includes a zener device configured to limit the voltage to less than a predetermined value that is indicative of the capability level of the circuit board.

5. The system of claim 3, wherein the circuit board further includes a sample circuit that latches a digital value indicative of the voltage on the capability signal line.

6. The system of claim 5, wherein the circuit board further includes a hold circuit coupled to the sample circuit to receive the digital value and configured to maintain the capability signal line at a voltage indicated by the digital value when the voting circuit is disabled.

7. The system of claim 1, further comprising multiple circuit boards inserted in corresponding sockets and configured to limit the voltage on the capability signal line to a predetermined value that is indicative of the capability level of the corresponding circuit board, whereby the voltage on the capability signal line is determined by the circuit board having the lowest voltage limit.

8. The system of claim 1, wherein the backplane further includes a circuit to power the capability signal line at a voltage no higher than a predetermined voltage that is indicative of the capability level of the backplane.

9. The system of claim 1, wherein the circuit board includes:

a processor;

a memory coupled to the processor;

a bridge device coupled between the processor and the backplane; and

a long-term storage device coupled to the bridge device.

10. A computer system comprising:

a processor;

a memory coupled to the processor;

a peripheral bus;

a bridge device coupled between the processor and the peripheral bus; and

a long-term storage device coupled to the bridge device,

wherein the peripheral bus includes a capability signal line having a voltage that is limited to a predetermined voltage that is one of three or more predetermined voltages each being indicative of a different capability level.

11. The system of claim 10, further comprising:

one or more peripheral components coupled to the peripheral bus, wherein each peripheral component is configured to limit the voltage on the capability signal line to a corresponding predetermined voltage that is indicative of a corresponding capability level of the peripheral component.

12. The system of claim 11, wherein the capability level is the maximum bus clock frequency supported by the peripheral component.

13. The system of claim 11, wherein each of the peripheral components includes a voting circuit having a zener diode configured for a predetermined voltage corresponding to the capability level of the peripheral component.

14. The system of claim 11, wherein each peripheral includes a voting circuit that limits the voltage on the capability signal line when a peripheral bus reset signal is asserted.

15. A method of determining a maximum bus clock rate supported by various components, the method comprising:

coupling the components to a bus having a capability signal line;

supplying electrical current to the capability signal line, wherein each of the components limits a voltage on the capability signal line to no more than a predetermined voltage that is indicative of a maximum bus clock rate supported by the component, each predetermined voltage being one of a set of three or more predetermined voltages that are indicative of different maximum clock rates; and

setting a bus clock rate to the maximum clock rate associated with the voltage on the capability signal line.

16. The method of claim 15, further comprising:

asserting a bus reset signal while supplying electrical current to the capability signal line.

17. The method of claim 16, further comprising:

measuring the voltage on the capability signal line after asserting the bus reset signal; and

holding the voltage on the capability signal line at the predetermined voltage associated with the bus clock rate.

18. The method of claim 15, wherein the components include zener devices configured in accordance with the maximum bus clock rate supported by the components.

19. The method of claim 18, further comprising:

disabling the zener devices when a bus reset signal is de-asserted.

20. The method of claim 17, further comprising:

detecting a voltage held on the capability signal line while the bus reset signal is de-asserted; and

determining if the voltage held on the capability signal line is consistent with a bus capability of a newly added bus component.

21. The method of claim 20, further comprising:

allowing the newly added bus component to participate in bus transactions if the voltage held on the capability signal line is consistent with the bus capability of the newly added bus component.

22. The method of claim 20, further comprising:

preventing the newly added bus component from participating in bus transactions until the bus reset signal is next asserted.